A Low Quiescent Current 3.3V Operation Linear MMIC Power Amplifier for 5 GHz WLAN Applications

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Abstract — **We report a 5 GHz linear InGaP/GaAs HBT monolithic microwave integrated circuit (MMIC) power amplifier for wireless LAN applications. The three-stage power amplifier operates with 103 mA – low quiescent current of Class AB mode using active bias circuit under a single supply of +3.3V. A total current of 196(194) mA is consumed with an output power of 18 dBm and PAE (power-added efficiency) of 9.7 % at 5.25(5.15) GHz. The power amplifier exhibits a power gain of 19.6 (17.8/18.5) dB, 1-dB compression point (P_1dB) of 26(25/25) dBm, and PAE of 27.8(25.4/20) % at 5.25(5.15/5.85) GHz. Measured third-order IMD(intermodulation distortion) is less than -25 dBc at 3 dB back-off and less than -30 dBc at 5 dB back-off from P_1dB for the frequency range between 5.15 and 5.85 GHz.**

I. Introduction

Wireless LAN(WLAN) applications have lately attracted considerable attention since the high data rate transmission and easy use for wireless Internet service are provided. At 5GHz frequency (U-NII band), the IEEE 802.11a and high performance radio LAN (HIPERLAN) 2 were developed as standards [1]-[2]. Both IEEE 802.11a and HIPERLAN2 employ orthogonal frequency division multiplexing (OFDM) modulation providing many advantages such as high data rates, the robustness to multi-path fading, and almost eliminated inter-symbol interference [3]. However, the large peak-to-average power ratio (PAPR) of OFDM signal is a serious problem causing signal distortion that occurs at a nonlinear region of the power amplifier. Therefore, the power amplifier should be driven in a very high linear output that is at least 6 dB back-off from P_1dB. In addition, the high efficiency is essential for long lifetime of battery when the power amplifier is used in NIC (Network Interface Card) of a laptop computer.

There were several reports on MMIC power amplifiers for 5 GHz WLAN applications. Some GaAs MMIC power amplifiers operate in Class A mode under 5V or 3.3V supply to meet the linearity requirement [4]-[6] and others operate in Class AB mode under 3V supply to improve the efficiency [7]. For applications to portable terminals the power amplifier needs to be operated with a single supply of 3.3V and requires consuming a low average dc current at the back-off output power while the linearity of the power amplifier is satisfied. To obtain simultaneously high linearity and efficiency, the power amplifier must be operated in Class AB mode under a single supply of 3.3V incorporating proposed linearizer.

In this paper, a 5 GHz linear InGaP/GaAs HBT MMIC power amplifier is developed for the frequency range between 5.15 and 5.85 GHz, including on chip active bias circuit for linearization, featuring a single supply of 3.3V, 103 mA-low quiescent current for the high efficiency, and P_1dB of more than 25 dBm. A fabricated chip size is as small as 1.4 X 0.8 mm^2 including input/inter-stage matching network and active bias circuits.

II. A Low Quiescent Current Biasing Scheme

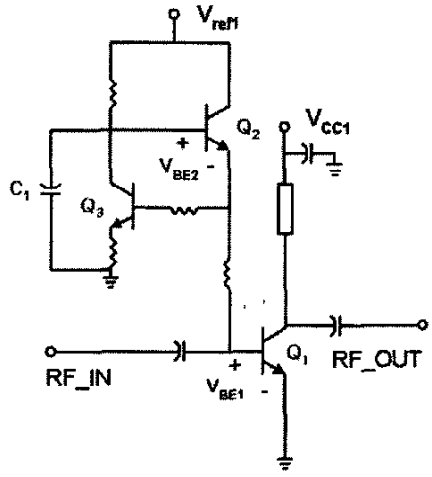

Fig. 1. Current mirror base bias circuit for a low quiescent current operation.

In order to achieve the low quiescent current, each stage of power amplifier was designed with a base bias circuit for Class AB mode operation. The current mirror base bias circuit including bypass capacitor is shown in Fig. 1. This bias circuit provides a constant base bias voltage of the power transistor Q_1 that decreases when the RF signal

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increases. The large RF signal is clipped through the base-emitter junction diode of HBT Q_2 and bypass capacitor C_1. Therefore, the base bias current of HBT Q_2 increases but the base bias voltage decreases with the increasing RF signal. As a result, the base bias voltage of power transistor Q_1 is compensated tracking the decrease of base-emitter junction voltage (V_{BE2}) of Q_2 [8]. With an aid of the base bias circuit, the bias point of the power transistor Q_1 is established in Class AB mode that uses a lower quiescent current than that of Class A mode. In this work, a low quiescent current for improved efficiency is applied to each of the three-stage power amplifier. The base bias circuit composed of the current mirror circuit and bypass capacitor provides improved current driving capability even in the high output power range.

III. Circuit Design Of MMIC Power Amplifier

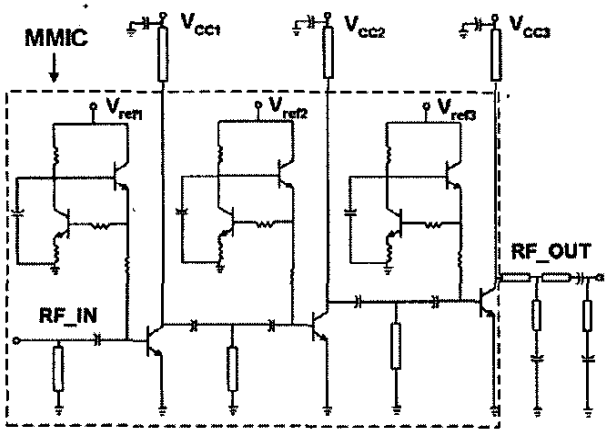

Fig. 2. Schematic of the three-stage InGaP/GaAs MMIC power amplifier for WLAN applications.

Fig. 2 shows a schematic of the three-stage InGaP/GaAs HBT MMIC power amplifier with the base bias circuit for WLAN applications. In order to obtain high gain and improved low frequency stability the high pass matching network is used at the input of each stage. The bypass capacitor, emitter area of the bias transistor of driver amplifier, 1st power amplifier, and 2nd power amplifier are optimized to maximize the linearity. The inter-stage matching network is implemented with a microstrip line on the GaAs substrate for the accuracy and low loss of the complex conjugate matching between the stages. The off-chip output matching network is composed of the shunt capacitor and microstrip line for the harmonic suppression.

A photograph of the developed InGaP/GaAs HBT MMIC power amplifier is shown in Fig. 3. Each bias circuit together with the matching networks for input and inter-stage is integrated in the MMIC, and the chip size is as small as 1.4 X 0.8 mm^2. Each of emitter area in the driver amplifier, 1st power amplifier, and 2nd power amplifier is 480 um^2, 1,440 um^2, and 2,880 um^2, respectively. In order to improve the stability and prevent the thermal run away, an emitter ballasting resistor is employed for each unit HBT in the driver amplifier and 1st power amplifier, and a base and an emitter ballasting resistors are also employed for the 2nd power amplifier.

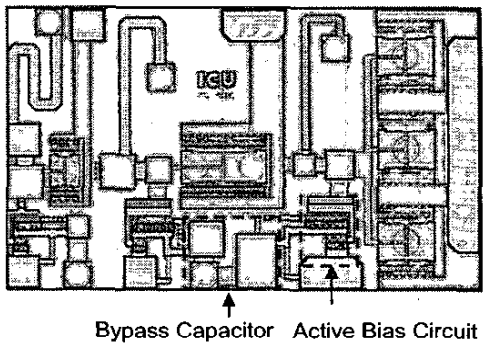

Fig. 3. Chip Photograph of the fabricated InGaP/GaAs HBT MMIC power amplifier.

IV. Measured Performance

S_{21} of the three-stage power amplifier depending on the various quiescent currents is shown in Fig. 4. S_{21} with a quiescent current of as low as 86 mA is over 16.3 dB and S_{21} with that of as high as 139 mA is also over 19.5 dB between 5.15 GHz and 5.85 GHz.

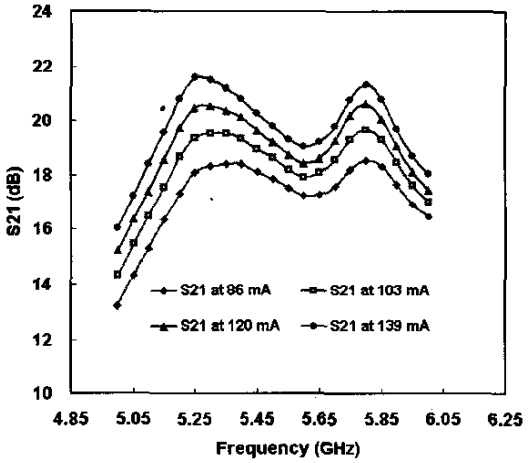

Fig. 4. Measured S_{21} in accordance with the various quiescent current levels.

Measured output power, power gain, and PAE with a single supply voltage of 3.3 V at both 5.25 and 5.15 GHz are shown in Fig. 5. The power amplifier uses a quiescent

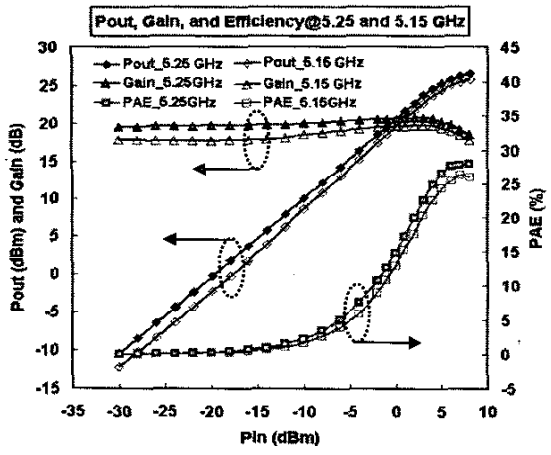

Fig. 5. Measured output power, gain and PAE with a single supply of 3.3 V at 5.25 and 5.15 GHz.

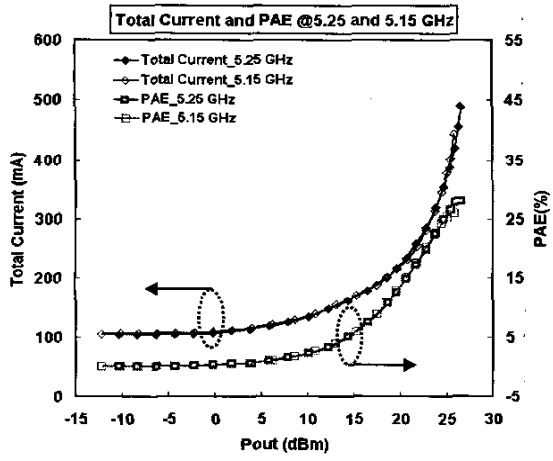

Fig. 6. Measured total current and PAE with a single supply of 3.3 V at 5.25 and 5.15 GHz.

current of 103 mA while providing a power gain of 19.6 (17.8) dB, P_1dB of 26 (25) dBm, and PAE of 27.8(25.4) % at 5.25 (5.15) GHz. Fig. 6 exhibits the total current and PAE in accordance with an output power. Because the power amplifier uses a low quiescent current of Class AB mode in this work, at 8 dB back-off output power of 18dBm that is standardized by IEEE 802.11a (5.25GHz), the total currents of 196 and 194 mA are achieved with PAE of 9.7 % through a CW power measurement. The performance of the power amplifier operating at 5.85 GHz is shown in Fig. 7. The power amplifier at 5.85 GHz delivers P_1dB of 25 dBm providing a power gain of 18.5 dB and PAE of 20 %. The total current consumption with an output power of 18 dBm is 244 mA with PAE of 7.4 % in Fig. 8.

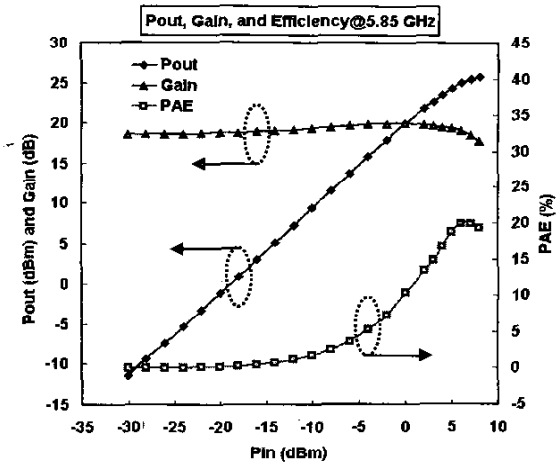

Fig. 7. Measured output power, gain and PAE with a single supply of 3.3 V at 5.85 GHz.

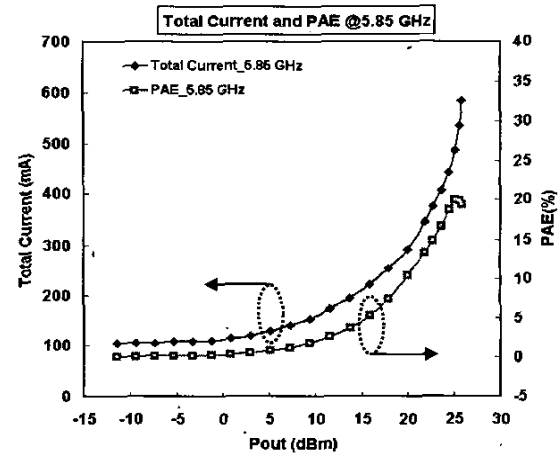

Fig. 8. Measured total current and PAE with a single supply of 3.3 V at 5.85 GHz.

As shown in Fig. 9 the measured third-order IMD which is frequency-dependent distortion is less than –25 dBc at 3 dB back-off and less than –30 dBc at 5 dB back-off from P_1dB for the frequency range between 5.15 and 5.85 GHz. Two-tone signals of 5 MHz offset frequency are used for the measurement of IMD. The IMD cancellation is observed near an output power of 20 dBm while operating in Class AB mode.

The power amplifier performance is summarized in Table 1. Harmonics of 2fo and 3fo are more than 60 and 37 dBc at P_1dB, respectively. Reverse isolation is also more than 31 dB at 5 GHz frequency range.

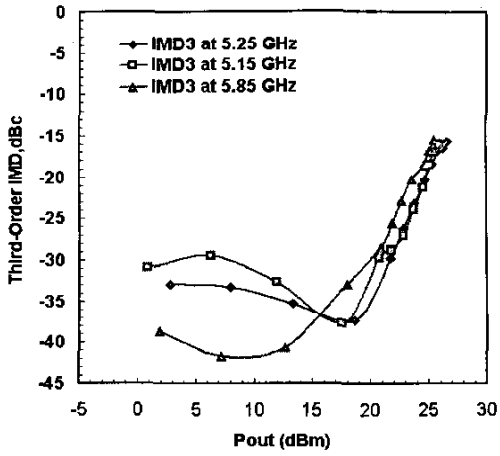

Fig. 9. Measured third-order IMD corresponding to the output power at between 5.15 and 5.85 GHz.

Table 1. Power Amplifier Performance Summary

Parameter	Measured data	
Frequency	5.15 ~ 5.85 GHz	
Supply Voltage	3.3 V	
Quiescent current	103 mA	
Gain	17 ~ 19 dB	
Output P_1dB	26/25/25 dBm	5.25/5:15/5.85 GHz
Total Current (at P_{OUT} of 18 dBm)	196/194/244 mA	
Third-order IMD	> 25(30) dBc at 3(5) dB back off from P_1dB	
Harmonics (2fo, 3fo)	> 60, 37 dBc at P_1dB	
Reverse Isolation	> 31 dB	

V. Conclusion

This paper demonstrates a 5 GHz linear InGaP/GaAs HBT MMIC power amplifier for wireless LAN applications using active bias circuit for linearization. The three-stage power amplifier operates with the 103 mA-low quiescent current of Class AB mode under a single supply of +3.3V. A total current of 196 and 194 mA is consumed for an output power of 18 dBm and PAE of 9.7 % at 5.25 and 5.15 GHz. The power amplifier exhibits a power gain of 19.6 (17.8/18.5) dB, P_1dB of 26(25/25) dBm, and PAE of 27.8(25.4/20) % at 5.25(5.15/5.85) GHz. Measured third-order IMD is less than -25 dBc at 3 dB back off and less than -30 dBc at 5 dB back off from P_1dB for the frequency range between 5.15 and 5.85 GHz.

Acknowledgement

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References

[1] "Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) Specifications: High-speed Physical Layer in the 5 GHz Band," September 1999.

[2] "Broadband Radio Access Networks(BRAN) HIPERLAN Type2; Physical (PHY) layer," 2000, ETSI TS 101 475.

[3] Richard van Nee and Ramjee Prasad, *OFDM for Wireless Multimedia Communications*, Artech House, 2000.

[4] A. Raghavan, E. Gebara, C-H. Lee, S. Chakraborty, D. Mukherjee, J. Bhattacharjee, D. Heo, J. Laskar, "A GaAs HBT 5.8 GHz OFDM transmitter MMIC chip set," *2001 IEEE RFIC Symp. Dig*, pp. 267 –270, June 2001.

[5] S. Chakraborty, C.-H. Lee, S. Yoo, D. Heo, A. Raghavan, D. Mukherjee, J. Bhattacharjee, J. Laskar, "A GaAs Based High Performance Transceiver Front-end Chipset for 5-6 GHz Wireless Applications," *2001 Radio and Wireless Conference*, pp. 25-28, August 2001.

[6] Thomas A.Bös and Urs Lott, "A Monolithic Integrated, On Chip Matched GaAs Power amplifier for HIPERLAN with a Single 3.3V Supply," *1996 26th European Microwave Conference*, pp. 191-194, September 1996.

[7] Y. M. Ikeda, M. Nagaoka, H. Wakimoto, T. Seshita, M. Mihara, M. Yoshimura, Y. Tanabe, K. Oya, Y. Kitaura, N. Uchitomi, "Single 3-V Supply Operation GaAs Linear Power MESFET Amplifier for 5.8-GHz ISM Band Applications," *IEICE Trans. ELECTRON.*, vol. E82-C, no. 7, pp. 1086-1091, July 1999.

[8] Y. S. Noh and C. S. Park, "PCS/W-CDMA Dual-Band MMIC Power Amplifier With A Newly Proposed Linearizing Bias Circuit," *IEEE Journal of Solid-State Circuits*, vol. 37, no. 9, pp. 1096-1099, September 2002.